Nepal College of information technology

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| Level: Bachelor | Year/Semester – III/I | Full Marks: 50 |
| Programme: BELX | | Pass Marks: 22.5 |
| Course: Integrated Digital Electronics | | Time : 2hrs. |
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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. Draw and explain voltage transfer characteristics of BJT inverter with its Noise Margins, Transition Width and Logic Swing. 2. Draw the IIL Circuit with current injector for a Decoder with 3input variables. | 7  3 |
|  | 1. The gate G0 has a fan-out of 5. Plot the transfer characteristic for the gate G0. Calculate noise margins.      1. Draw the RTL circuit for Ex-OR gate and explain its operation. | 7  3 |
|  | 1. For the DTL NAND gate shown below, assume VCE (sat) = 0.2V, VBE(on) VD(on) = 0.8V and ßF = 50.Calculate Fan Out for output "High"      1. Draw the standard TTL NAND Gate circuit. Explain its operation. Also discuss the use of the totem-pole pair, multiemitter transistor and the diode in the circuit. | 7  8 |
|  | Write short notes on**:**   1. High Threshold Logic 2. Comparison between DTL and TTL 3. Active Pull UP. | 3×5 |